CLAIMS

We claim:

1. A flash memory device, comprising:

a memory cell array block including a plurality of flash memory cells;

a program verify voltage generating unit capable of variably generating a program verify voltage that verifies flash memory cells programming;

a wordline level selecting unit capable of transferring the program verify voltage to the flash memory cells; and

a page buffer including a latch capable of storing data of the flash memory cells and resetting the latch whenever the program verify voltage is lowered.

2. The flash memory device of claim 1 where the program verify voltage generating unit includes:

a PMOS transistor coupled at a first end to a power supply voltage;

first to third resistors serially coupled between a second end of the PMOS transistor and a ground voltage;

a first NMOS transistor coupled across the first resistor and responsive to a first program verify control signal, the first NMOS transistor generating a program verify voltage;

a second NMOS transistor coupled across the second resistor responsive to a second program verify control signal; and

a comparator capable of comparing a voltage at a node between the first and second resistors with a reference voltage, the comparator having an output connected a gate of the PMOS transistor.

3. The flash memory device of claim 2 where the first and second program verify control signals are selectively activated to thereby fluctuate the program verify voltage.

4. The flash memory device of claim 1 where the wordline level selecting unit applies a program voltage, a read voltage, and a pass voltage or an erase voltage to a wordline.

5. The flash memory device of claim 1 where the page buffer includes:

a first NMOS transistor coupled to the flash memory cells and responsive to a first bitline control signal;

a first PMOS transistor coupled to the first NMOS transistor and capable of precharging a sensing node to a predetermined voltage level responsive to a precharge signal;

a second NMOS transistor coupled to the sensing node and gates to a second bitline control signal;

a latch coupled to the second NMOS transistor and capable of latching the voltage at the sensing node;

a third NMOS transistor coupled to the latch and responsive to the voltage at the sensing node;

a fourth NMOS transistor coupled between the third NMOS transistor and a ground voltage and capable of storing the flash memory cell data in the latch responsive to a first latch control signal; and

a fifth NMOS transistor coupled between the sensing node and a ground voltage and capable of resetting the sensing node responsive to a bitline reset signal.

6. The flash memory device of claim 5 where the page buffer includes:

a sixth NMOS transistor capable of transferring data inputted in a program operation of the flash memory device responsive to a data loading enable signal;

a second latch capable of storing the inputted data;

a seventh NMOS transistor coupled to the second latch and responsive to the voltage level at the sensing node;

an eighth NMOS transistor coupled between the seventh NMOS transistor and a ground voltage and capable of latching the inputted data to the second latch responsive to a second latch control signal; and

a ninth NMOS transistor coupled between the first latch and the fourth NMOS transistor and responsive to the inputted data.

7. A method of verifying flash memory cell programming, comprising:

applying a predetermined program voltage to a plurality of flash memory cells;

generating a program verify voltage in selective response to program verify control signals;

verifying flash memory cell programming responsive to the program verify voltage;

repeating, applying, generating, and verifying when the flash memory cells are programmed;

maintaining the program verify voltage uniform during predetermined program unit loop cycles; and

storing the flash memory cell data in a latch at each program unit loop cycle where the program verify voltage level is lowered.

8. The method of claim 7 comprising initially applying a voltage higher than the threshold voltage of the flash memory cells as the program verify voltage.

9. The method of claim 7 comprising increasing the program voltage at each program unit loop.